

What is claimed is:

1. A circuit comprising:

a reference current source to provide a substantially noise free differential current signal; and

a detector coupled to one or two power supplies, the detector to receive the substantially noise free differential current signal, to detect a noise signal on the one and/or two power supplies, and to generate a high noise detection signal to indicate detection of the noise signal.

2. The circuit of claim 1, wherein the detector comprises:

a PMOS current mirror to receive the substantially noise free differential current signal;

an NMOS current mirror to receive a substantially noise free complementary current signal;

a first resistor coupled to the PMOS current mirror;

a second resistor coupled to the NMOS current mirror;

a comparator coupled to the current mirrors and the resistors;

two resistor-capacitor high-pass filters, each coupled to one of the two comparator's inputs;

one or more capacitors, each of the one or more capacitors coupled to at least one of the two power supplies and to a resistor-capacitor high-pass filter via a NMOS switch;

a filter load, comprising selectable low-pass filter paths, each path comprising pass-gates and a resistor-capacitor low-pass filter, the filter load is coupled to the comparator;

a Schmitt trigger coupled to the filter load, the Schmitt trigger to generate the pre-noise detection signal;

an exclusive-OR gate coupled to the Schmitt trigger, to provide noise polarity selection;

20 a logic-high latch comprising a NOR gate, a NAND gate, and three inverters, to  
21 store the high noise detection signal, and to reset the high noise detection signal; and  
22 a flip-flop register coupled to the logic-high latch to synchronize the high noise  
23 detection signal.

1 3. The circuit of claim 1, wherein the reference current source comprises:  
2 a substantially noise free ground;  
3 a control signal source;  
4 a voltage reference coupled to the substantially noise free ground;  
5 a voltage follower differential amplifier coupled to the substantially noise free  
6 ground and to the voltage reference;  
7 a PMOS-NMOS-NMOS diode stack coupled to the voltage follower differential  
8 amplifier and to the substantially noise free ground;  
9 Controllable NMOS current scalars coupled to the substantially noise free ground  
10 signal source, the control signal source, and the diode stack, and a PMOS transistor load,  
11 to provide a calibration voltage for controllable PMOS current scalars;  
12 NMOS current mirrors coupled to the controllable PMOS current scalars and the  
13 substantially noise free ground to provide the substantially noise free reference current  
14 signal; and  
15 PMOS current mirrors coupled to a NMOS current mirrors, and the substantially  
16 noise free ground, to provide the substantially noise free complementary reference  
17 current signal.

1 4. The circuit of claim 3, wherein the voltage reference comprises a bandgap voltage  
2 reference.

- 1        5.        A circuit comprising:  
2                a plurality of reference current sources formed on a substrate, each of the plurality  
3        of reference current sources to provide a substantially noise free differential current  
4        signal; and  
5                a plurality of detectors formed on the substrate, each of the plurality of detectors  
6        coupled to one or two power supplies, each of the plurality of detectors to receive the  
7        substantially noise free differential current signal and to detect a noise signal on the one  
8        or two power supplies and to generate a noise detection signal to indicate detection of the  
9        noise signal.
- 1        6.        The circuit of claim 5, wherein the substrate comprises silicon.
- 1        7.        The circuit of claim 6, wherein each of the plurality of detectors comprises a  
2        comparator.
- 1        8.        The circuit of claim 7, wherein each of the comparators comprises complementary  
2        metal-oxide semiconductor field-effect transistors.
- 1        9.        The circuit of claim 5, wherein the substrate comprises gallium arsenide.
- 1        10.       The circuit of claim 6, wherein each of the plurality of reference current sources  
2        comprises a pair of complementary current sources.
- 1        11.       The circuit of claim 5, wherein the substrate comprises silicon and germanium.
- 1        12.       The circuit of claim 11, wherein each of the plurality of reference current sources  
2        comprises a controllable current source.
- 1        13.       The circuit of claim 5, wherein the substrate comprises a processor.

1        14.     The circuit of claim 13, wherein the processor comprises a very-long instruction  
2        word processor.

1        15.     A method comprising:  
2                receiving a substantially noise free current signal;  
3                receiving one or two power supply signals;  
4                processing the substantially noise free current signal and the one or two power  
5        supply signals to detect a noise signal in the one or two power supply signals; and  
6                generating a noise detection signal in response to detection of the noise signal.

1        16.     The method of claim 15, wherein receiving the substantially noise free current  
2        signal comprises:  
3                receiving a pair of complementary current signals.

1        17.     The method of claim 15, wherein receiving the one or two power supply signals  
2        comprises:  
3                receiving two voltage signals having different polarities.

1        18.     The method of claim 15, wherein processing the substantially noise free current  
2        signal and the one or two power supply signals to detect the noise signal in the one or two  
3        power supply signals comprises:  
4                comparing the one or two power supply signals to the substantially noise free  
5        current signal.

1        19.     The method of claim 15, wherein generating the noise detection signal in response  
2        to detection of the noise signal comprises:  
3                generating a digital signal in response to detection of the noise signal.

- 1        20.    The method of claim 15, further comprising:
- 2                setting a calibration potential level; and
- 3                setting a noise-detection threshold level.